

WE CLAIM:

1. A semiconductor assembly comprising:

a strip-like flexible interconnector of electrically
insulating material having first and second
surfaces;

electrically conductive lines integral with said
interconnector, forming on said first surface a
first array of electrical entry ports and a
second array of exit ports, said arrays grouped
in separate areas of said interconnector;

said entry ports spaced apart by less, center to
center, than said exit ports are spaced apart,
center to center;

said interconnector folded so that said entry ports
face in one direction while said exit ports face
in the opposite direction;

at least one semiconductor device having a plurality
of first electrical coupling members, said first
coupling members attached to said entry ports;
and

a plurality of second electrical coupling members
attached to said exit ports, said second coupling
members suitable for attachment to other parts.

2. The assembly according to Claim 1 wherein said
semiconductor device is an integrated circuit chip
having an active and a passive surface, said first
coupling members attached to said active surface.

3. The assembly according to Claim 1 wherein said
semiconductor device is an integrated circuit chip
encapsulated in a package with outside contact pads,

said first coupling members attached to said contact pads.

4. The assembly according to Claim 1 further comprising at least one passive electrical component integrated into said conductive lines on said interconnector.
5. The assembly according to Claim 1 wherein said entry ports are spaced apart less than 100 μm center to center, and said exit ports are spaced apart more than 100 μm center to center.
- 10 6. The assembly according to Claim 1 wherein said interconnector is a flexible polyimide film.
7. The assembly according to Claim 1 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.
- 15 8. The assembly according to Claim 1 wherein said first and second coupling members are solder balls selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.
- 20 9. The assembly according to Claim 1 wherein said first coupling members are selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.
- 25 10. The assembly according to Claim 1 further having an adhesive non-conductive polymer underfilling any spaces between said first coupling members attached to said entry ports under said semiconductor device.
- 30 11. A semiconductor assembly comprising:
 - a strip-like flexible interconnector of electrically insulating material having first and second

surfaces;

said interconnector having on said first surface
electrically conductive lines for connecting a
a plurality of semiconductor devices formed on
said first surface adjacent to each other;

said interconnector further having electrically
conductive paths extending through said
interconnector from said first surface to said
second surface, forming at least one array of
electrical ports on said second surface;

said interconnector folded so that said adjacent
semiconductor devices are stacked on top of each
other; and

a plurality of electrical coupling members attached
to said ports, said coupling members suitable for
attachment to other parts.

12. The assembly according to Claim 11 further comprising
at least one discreet passive electrical component
attached to said ports.

13. The assembly according to Claim 11 further comprising
at least one semiconductor device attached to said
ports.

14. The assembly according to Claim 11 further comprising
at least one passive electrical component integrated
into said conductive lines on said interconnector.

15. A semiconductor assembly comprising:
a strip-like flexible interconnector of electrically
insulating material having first and second
surfaces;

said interconnector having on said first surface
electrically conductive lines for connecting a
plurality of semiconductor devices formed on said

first surface adjacent to each other;
said interconnector further having electrically
conductive paths extending through said
interconnector from said first surface to said
5 second surface, forming electrical ports on said
second surface;

said ports comprise first and second pluralities,
said first plurality ports spaced apart by less,
center to center, than said second plurality
10 ports are spaced apart, center to center;

said interconnector folded so that said adjacent
semiconductor devices are stacked on top of each
other;

at least one additional semiconductor device having
15 a plurality of first electrical coupling members,
said first coupling members attached to said
first plurality ports; and

a plurality of second electrical coupling members
attached to said second plurality ports, said
20 coupling members suitable for attachment to other
parts.

16. A method of assembling an integrated circuit device,
comprising the steps of:

forming electrically conductive lines on a strip-
25 like flexible interconnector of electrically
insulating material having first and second
surfaces;

forming on said first surface a first array of
electrical entry ports and a second array of
30 exit ports, said arrays grouped in separate
areas of said interconnector, said entry ports
spaced apart by less, center to center, than

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said exit ports are spaced apart, center to center;

attaching at least one semiconductor device having a plurality of first electrical coupling members to said entry ports;

attaching a plurality of second electrical coupling members to said exit ports; and

folding said interconnector so that said entry ports face in one direction while said exit ports face in the opposite direction.

17. The method according to Claim 16 further comprising the step of:

integrating at least one passive electrical component into said conductive lines on said interconnector.

18. The method according to Claim 16 further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said first coupling members attached to said entry ports under said semiconductor device.

19. A method of assembling an integrated circuit device, comprising the steps of:

forming electrically conductive lines on a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

forming electrically conductive paths extending through said interconnector from said first surface to said second surface, forming at least one array of electrical ports on said second surface;

forming on said first surface a plurality of
semiconductor devices adjacent to each other and
connected to said conductive lines;
attaching a plurality of electrical coupling members
5 to said ports; and
folding said interconnector so that said adjacent
semiconductor devices are stacked on top of each
other.

20. The method according to Claim 19 further comprising the
10 step of:

attaching at least one discreet passive electrical
component to said ports.

21. The method according to Claim 19 further comprising the
step of:

15 attaching at least one semiconductor device to said
ports.

22. The method according to Claim 19 further comprising the
step of:

20 integrating at least one passive electrical
components into said conductive lines on said
interconnector.

23. A method of assembling an integrated circuit device,
comprising the steps of:

25 forming electrically conductive lines on a strip-
like flexible interconnector of electrically
insulating material having first and second
surfaces;
forming electrically conductive paths extending
through said interconnector from said first
30 surface to said second surface, forming
electrical ports on said second surface such that
said ports comprise first and second pluralities,

said first plurality ports spaced apart less,
center to center, than said second plurality
ports are spaced apart, center to center;
forming on said first surface a plurality of
5 semiconductor devices adjacent to each other and
connected to said conductive lines;
attaching at least one additional semiconductor
device, having a plurality of first electrical
coupling members, to said first plurality ports;
10 attaching a plurality of second electrical coupling
members to said second plurality ports; and
folding said interconnector so that adjacent
semiconductor devices are stacked on top of each
other.

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